ACM International Conference on Computing Frontiers 2017

May 15 - 17, 2017, Siena, Italy

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ACM International Conference on Computing Frontiers 2017

May 15 - 17, 2017, Siena, Italy

Keynotes

room: Aula Magna (2nd floor)

Keynote 1 - Runtime Aware Architectures

Mateo Valero, Computer Architecture Department — UPC Barcelona

Abstract:

In the last years the traditional ways to keep the increase of hardware performance to the rate predicted by the Moore's Law vanished. When uni-cores were the norm, hardware design was decoupled from the software stack thanks to a well defined Instruction Set Architecture (ISA). This simple interface allowed developing applications without worrying too much about the underlying hardware, while computer architects proposed techniques to aggressively exploit Instruction-Level Parallelism (ILP) in superscalar processors. Current multi-cores are designed as simple symmetric multiprocessors on a chip. While these designs are able to compensate the clock frequency stagnation, they face multiple problems in terms of power consumption, programmability, resilience or memory. The solution is to give more responsibility to the runtime system and to let it tightly collaborate with the hardware. The runtime has to drive the design of future multi-cores architectures. In this talk, we introduce an approach towards a Runtime-Aware Architecture (RAA), a massively parallel architecture designed from the runtime's perspective.

Bio:

Mateo Valero is a professor in the Computer Architecture Department at UPC, in Barcelona. His research interests focuses on high performance architectures. He has published approximately 700 papers, has served in the organization of more than 300 International Conferences and he has given more than 500 invited talks. He is the director of the Barcelona Supercomputing Centre, the National Centre of Supercomputing in Spain.

Dr. Valero has been honoured with several awards. Among them, Seymour Cray Award, one of the IEEE Computer Society's highest awards in contributions to high-performance computing; the Eckert-Mauchly Award, one of the IEEE-ACM highest awards in contributions to computer architectures; Harry Goode Award; ACM Distinguished service; Euro-Par Achievement Award; the "King Jaime I" in research and two National Awards on Informatics and on Engineering. He has been named Honorary Doctor by 9 Universities. "Hall of the Fame" member of the IST European Program (selected as one of the 25 most influents European researchers in IT during the period 1983-2008. Lyon, November 2008).

Fellow of IEEE, ACM, Intel Distinguished Research Fellow. Member of Royal Spanish Academy of Engineering, Royal Academy of Science and Arts, correspondent academic of Royal Spanish Academy of Sciences, Academia Europaea and Mexican Academy of Science.

In 1998 he won a "Favourite Son" Award of his home town, Alfamén (Zaragoza) and in 2006, his native town of Alfamén named their Public College after him.

Keynote 2 - The Future of Deep Learning: Challenges & Solutions

Mark Robins, Intel Nervana

Abstract:

Mark will begin with a brief overview of deep learning and what has led to its recent popularity. He will provide a few demonstrations and examples of deep learning applications based on recent work at Intel Nervana.

He will explain some of the challenges to continued progress in deep learning — such as high compute requirements and lengthy training time — and will discuss some of the solutions (e.g. custom deep learning hardware) that Intel Nervana is developing to usher in a new era of even more powerful AI.

Bio:

Mark Robins is Head of Products for Intel Nervana where he is responsible for the Nervana Deep Learning Platform. The Nervana DL Platform, available on both Nervana Cloud and the Nervana DL Appliance, includes the Nervana DL Software Suite, the neon deep learning framework, and the Nervana Engine, a processor that has been custom-designed and optimized for deep learning. Businesses and researchers use the Nervana DL Platform to develop and deploy custom, enterprise-grade deep learning solutions at a fraction of the cost of building their own infrastructure and data science team. Nervana was acquired by Intel in August 2016.

Prior to Nervana, Mark served as VP Product for Influitive and, before that, as VP Product for Chegg through their IPO in 2013. Before Chegg, Mark was co-founder/CEO of Grouply, a social networking startup funded by Reid Hoffman and O'Reilly Alphatech Ventures that was acquired in 2010. Before Grouply, Mark was Sr. Director of Product Management at Siebel Systems through its acquisition by Oracle in 2006. Mark started his career as a satellite communications systems engineer for Hughes Aircraft Company, which is now part of Boeing. Mark earned a BS and MS in electrical engineering from Cornell and Caltech, respectively, where he also studied neural networks. Mark holds an MBA from Harvard Business School.

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Conference Programme

	Monday May 15		Tuesday May 16		Wednesday May 17
08:30	08:30-08:45 Welcome & Opening Remarks				
08:45	08:45-09:45 Keynote 1		08:45-09:45 Keynote 2		08:45-10:00 Cloud Computing & Virtualization
09:45	09:45-10:30 Panel 1		09:45-10:30 Panel 2		
10:05					10:05-10:55 Runtime Techniques
10:30	(break)		(break)		
10:55					(break)
11:00	11:00-12:15 Programming Systems	11:00-13:00 Big Data Analytics Workshop	11:00-12:40 Applications at the Frontier	11:00-12:40 Design of Low Power Embedded Systems	
11:25					11:25-13:05 Compiler & Scheduling Techniques
12:20	12:20-13:00 Short Papers 1				
12:40			(lunch)		
13:00	(lunch)				
13:05					(lunch)
13:40			13:40-15:00 Special Session on Collaborative Projects		
14:00	14:00-14:40 Short Papers 2				
14:05					14:05-15:20 Memory Performance
14:45		14:00-16:00 Malicious Software and Hardware in Internet of Things			
15:05	14:45-16:00 Trusted Execution		15:05-15:55 GPUs & Accelerators (1)	15:05-15:55 Special Session on Industrial Views	
15:20					
15:55			(break)	(break)	
16:00	(break)	(break)			
16:15			16:15-17:30 GPUs & Accelerators (2)	16:15-17:30 Special Session on Industrial Views	
16:30	16:30-17:40 Short Papers 3	16:30-17:30 Malicious Software and Hardware in Internet of Things			15:20-15:50 Closing Remarks
17:30			17:30-23:30 Guided Tour and Conference Banquet		
17:40	17:40-19:00 Welcome Cocktail & Poster Session				

Monday May 15

08:30-08:45	**Welcome & Opening Remarks**
08:45-09:45	**Keynote 1** Chair: Francesca Palumbo
	Runtime Aware Architectures Mateo Valero (Barcelona Supercomputing Center)
09:45-10:30	**Panel 1**
	Hardware/Software Interaction: the Missing Piece
10:30-11:00	(break)

Parallel Track I ***room: Aula Magna (2nd floor)***

11:00-12:15	Session **Programming Systems**
11:00-12:15	StreamDrive: A Dynamic Dataflow Framework For Clustered Embedded Architectures Arthur Stoutchinin and Luca Benini
11:25-11:50	Quality Optimization of Resilient Applications under Temperature Constraints Heng Yu, Yajun Ha and Jing Wang
11:50-12:15	DYCE - A Resilient Shared Memory Paradigm for Heterogenous Distributed Systems without Memory Coherence Ulrich Finkler, Hubertus Franke and David Kung
12:20-13:00	Session **Short Papers 1** Chair: Miquel Moreto
12:20-12:30	Analytical Performance Modeling and Validation of Intel's Xeon Phi Architecture Sudheer Chunduri, Prasanna Balaprakash, Vitali Morozov, Venkat Vishwanath and Kalyan Kumaran
12:30-12:40	Using Personality Metrics to Improve Cache Interference Management in Many-Core Processors Mwaffaq Otoom, Aamer Jaleel and Pedro Trancoso

12:40-12:50	Selective off-loading to Memory: Task Partitioning and Mapping for PIM-enabled Heterogeneous Systems Yi Liao, Ying Wang, Dawen Xu, Huawei Li and Xiaowei Li

Parallel Track II ***room: Aula Magna Storica (1st floor)***

11:00-13:00	Session **Big Data Analytics Workshop**
13:00-14:00	(lunch)

Parallel Track I ***room: Aula Magna (2nd floor)***

14:10-14:40	Session **Short Papers 2** Chair: Miquel Moreto
14:10-14:20	Large-Scale Plant Classification with Deep Neural Networks Ignacio Heredia
14:20-14:30	Software-defined Networks in large-scale radio telescopes P. Chris Broekema, Damiaan R. Twelker, Daniel C. Romão, Paola Grosso, Rob V. van Nieuwpoort and Henri E. Bal
14:30-14:40	Evolution of Friendship: a case study of MobiClique Jooyoung Lee, Konstatin Lopatin, Rasheed Hussain and Waqas Nawaz
14:45-16:00	Session **Trusted Execution** Chair: Davide Ariu
14:45-15:10	RAGuard: A Hardware Based Mechanism for Backward-Edge Control-Flow Integrity Jun Zhang, Rui Hou, Junfeng Fan, Ke Liu, Lixin Zhang and Sally A. McKee
15:10-15:35	SGXKernel: A Library Operating System Optimized for Intel SGX Hongliang Tian, Yong Zhang, Chunxiao Xing and Shoumeng Yan
15:35-16:00	Data mining the memory access stream to detect anomalous application behavior Francis Moreira, Matthias Diener, Philippe Navaux and Israel Koren
16:00-16:30	(break)
16:30-17:40	Session **Short Papers 3** Chair: Miquel Moreto

16:30-16:40 A Resource-aware Malleable Tsunami Simulation Realized on an Elastic MPI Infrastructure
Ao Mo-Hellenbrand, Isaías A. Comprés Ureña, Oliver Meister, Hans-Joachim Bungartz, Michael Gerndt and Michael Bader

16:40-16:50 Peak load optimization through 2-dimensional packing and multi-processor real-time scheduling
Daniele De Martini, Guido Benetti, Filippo Cipolla, Davide Caprino, Marco Luigi Della Vedova and Tullio Facchinetti

16:50-17:00 Cloud Workload Prediction by Means of Simulation
Gabor Kecskemeti, Attila Kertesz and Zsolt Nemeth

17:00-17:10 Hardware Support for Secure Stream Processing in Cloud Environments
Jeff Anderson and Tarek El-Ghazawi

17:10-17:20 Let's Go: a Data-Driven Multi-Threading Support
Alberto Scionti and Somnath Mazumdar

17:20-17:30 Brain-Inspired Data-Driven Architecture for Sparse Nonlocal and Unstructured Workloads
Yasunao Katayama

17:30-17:40 CAROL-FI: an Efficient Fault-Injection Tool for Vulnerability Evaluation of Modern HPC Parallel Accelerators
Daniel Alfonso Gonçalves De Oliveira, Vinícius Fratin Netto, Philippe Navaux, Israel Koren and Paolo Rech

Parallel Track II — *room: Aula Magna Storica(1st floor)*

14:00-16:00	Session **Malicious Software and Hardware in Internet of Things**
16:00-16:30	(break)
16:30-17:30	Session **Malicious Software and Hardware in Internet of Things**

Plenary Session

17:40-19:00 **Welcome Cocktail & Poster Session**

Tuesday May 16

08:45-09:45	**Keynote 2** Chair: Michela Becchi Future of Deep Learning: Challenges & Solutions Mark Robins (Intel)
09:45-10:30	**Panel 2** Designing Cyber-Physical Systems: Incremental Approaches or Disruptive Technologies?
10:30-11:00	(break)

Parallel Track I ***room: Aula Magna (2nd floor)***

11:00-12:40	Session **Applications at the Frontier** Chair: John Feo
11:00-11:25	A Holistic Approach for Implementing Neural Network Computations Matthew Moskewicz, Ali Jannesari and Kurt Keutzer
11:25-11:50	Finding Maximum Cliques Using Quantum Annealing Guillaume Chapuis, Hristo Djidjev, Georg Hahn and Guillaume Rizk
11:50-12:15	An Ensemble Model for Diabetes Diagnosis in Large-scale and Imbalanced Dataset Xun Wei, Fan Jiang, Feng Wei, Jiekui Zhang, Weiwei Liao and Shaoyin Cheng
12:15-12:40	Self-sustainability in Nano Unmanned Aerial Vehicles: A Blimp Case Study Daniele Palossi, Andres Gomez, Stefan Draskovic, Kevin Keller, Luca Benini and Lothar Thiele

Parallel Track II ***room: Aula Magna Storica(1st floor)***

11:00-12:40	Session **Design of Low Power Embedded Systems**
12:40-13:40	(lunch)

Plenary Session

13:40-15:00	Session **Special Session on Collaborative Projects** Chair: Francesca Palumbo
13:40-14:00	BONSEYES: Platform for Open Development of Systems of Artificial Intelligence Tim Llewellynn, et al.
14:00-14:20	Designing Swarms of Cyber-Physical Systems: the H2020 CPSwarm Project Alessandra Bagnato, et al.
14:20-14:40	HELICoiD: interdisciplinary and collaborative project for real-time brain cancer detection Rubén Salvador, et al.
14:40-15:00	Social Engineering 2.0: A Foundational Work Davide Ariu, et al.

Parallel Track I *room: Aula Magna (2nd floor)*

15:05-15:55	Session **GPUs & Accelerators (1)** Chair: Leandro Fiorin
15:05-15:30	Data Analytics with NVLink: An SpMV Case Study Daniele Buono, Fausto Artico, Fabio Checconi, Jee W. Choi, Xinyu Que and Lars Schneidenbach
15:30-15:55	An Enhanced Image Reconstruction Tool for Computed Tomography on GPUs Xiaodong Yu, Hao Wang, Wu-Chun Feng, Hao Gong and Guohua Cao
15:55-16:15	(break)
16:15-17:30	Session **GPUs & Accelerators (2)** Chair: Leandro Fiorin
16:15-16:40	GPU-UniCache: Automatic Code Generation of Spatial Blocking for Stencils on GPUs Kaixi Hou, Hao Wang and Wu-Chun Feng
16:40-17:05	High Performance Coordinate Descent Matrix Factorization for Recommender Systems Xi Yang, Jianbin Fang, Jing Chen, Chengkun Wu, Tao Tang and Kai Lu
17:05-17:30	Vectorization of Hybrid Breadth First Search on the Intel Xeon Phi Mireya Paredes Lopez, Graham Riley and Mikel Lujan

Parallel Track II *room: Aula Magna Storica(1st floor)*

15:05-15:55	Session **Special Session on Industrial Views** Chair: Antonino Tumeo
15:05-15:30	NSF Center for High-Performance Reconfigurable Computing (CHREC) Wu-Chun Feng
15:30-15:55	Designing and Programming the Configurable Cloud Andrew Putnam
15:55-16:15	(break)
16:15-17:30	Session **Special Session on Industrial Views** Chair: Antonino Tumeo
16:15-16:40	ARM HPC Ecosystem and the Reemergence of Vectors Alex Rico
16:40-17:05	Extending the Comfort Zone: DAVIDE Fabrizio Magugliani
17:05-17:30	Roundtable on Industrial Perspectives

Plenary Session

17:30-23:30	**Guided tour and Conference Banquet**

Wednesday May 17

08:45-10:00	Session **Cloud Computing & Virtualization**
08:45-09:10	Recommending Resources to Cloud Applications based on Custom Templates Composition Ronny Bazan Antequera, Prasad Calyam, Arjun Chandrashekara and Shivoam Malhotra
09:10-09:35	Advanced Manufacturing Collaboration in a Cloud-based App Marketplace Amit Rama Akula, Prasad Calyam, Ronny Bazan Antequera and Raymond Leto
09:35-10:00	Warm is Not Warm: Understanding the I/O Behavior of Desktop Applications in Virtualization Environments Yan Sui, Chun Yang and Xu Cheng
10:05-10:55	Session **Runtime Techniques** Chair: Hubertus Franke
10:05-10:30	Work Stealing in a Shared Virtual-Memory Heterogeneous Environment Shuai Che, Marc Orr and Jonathan Gallmeier
10:30-10:55	Designing Scalable Distributed Memory Models: A case study Joshua Landwehr, Joshua Suetterlein, Joseph Manzano, Andres Marquez, Kevin Barker and Guang R Gao
10:55-11:25	(break)
11:25-13:05	Session **Compiler & Scheduling Techniques** Chair: Josef Weidendorfer
11:25-11:50	Trading Fault Tolerance for Performance in AN Encoding Norman Rink and Jeronimo Castrillon
11:50-12:15	ExanaDBT: A Dynamic Compilation System for Transparent Polyhedral Optimizations at Runtime Yukinori Sato, Tomoya Yuki and Toshio Endo
12:15-12:40	Task-parallel Runtime System Optimization Using Static Compiler Analysis Peter Thoman, Peter Zangerl and Thomas Fahringer
12:40-13:05	Exploring the Performance Limits of Out-of-order Commit Mehdi Alipour, Trevor E. Carlson and Stefanos Kaxiras
13:05-14:05	(lunch)

14:05-15:20	Session **Memory Performance** Chair: Carsten Trinitis
14:05-14:30	Optimizing memory affinity with a hybrid compiler/OS approach Matthias Diener, Eduardo Cruz, Marco Antonio Zanata Alves, Edson Borin and Philippe Navaux
14:30-14:55	BC-AMAT: Considering Blocked Time in Memory System Measurement Qi Yu, Libo Huang, Cheng Qian and Zhiying Wang
14:55-15:20	Optimal On-Line Computation of Stack Distances for MIN and OPT Gianfranco Bilardi, Kattamuri Ekanadham and Pratap Pattnaik
15:20-15:50	**Closing Remarks**

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Workshops

room: Aula Magna Storica (1st floor)

Monday May 15 11:00 – 13:00 room: Aula Magna Storica (1st floor)

BigDAW17
Big Data Analytics Workshop

Sponsor

IBM Research | Zurich

Aim and scope

Managing and processing large volumes of data, or "Big Data", and gaining meaningful insights is a significant challenge facing the distributed computing community. As a consequence, many business are demanding large-scale streaming data analytics. This has a significant impact on a wide range of domains, including health care, bio-medical research, Internet searches, finance and business informatics, and scientific computing.

Despite considerable progress in high performance, storage capacity, and computation power, challenges remain in identifying, clustering, classifying, and interpreting a large spectrum of information.

The purpose of this workshop is to provide a fertile ground for collaboration among research institutions and industries in the fields of analytics, machine learning, and high-performance computing.

Topics of interest

- High-performance data analytics
- Machine and deep learning
- Data search and representation
- Architecture and system design
- Cloud-based Big Data solutions
- Software infrastructures

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  Oramon Labs, NL
- Christian Pilato
  University of Lugano, CH
- Annalisa Riccardi
  University of Strathclyde, UK
- Mark Thompson
  Leids Universitair Medisch Centrum, NL

Programme

11:00 - 11:20	"Towards Big Data Visualization for Monitoring and Diagnostics of High Volume Semiconductor Manufacturing"
	Dimitra Gkorou, Alexander Ypma, George Tsirogiannis, Manuel Giollo, Dag Sonntag, Geert Vinken, Richard van Haren, Robert Jan van Wijk, Jelle Nije, Tom Hoogenboom
	Speaker: Dimitra Gkorou, ASML
11:20 - 11:40	"Big Data Analytics on Large-Scale Scientific Datasets in the INDIGO-DataCloud Project"
	Sandro Fiore, Cosimo Palazzo, Alessandro D'Anca, Donatello Elia, Elisa Londero, Cristina Knapic, Stephen Monna, Nicola M. Marcucci, Fernando Aguilar, Marcin Płóciennik, Jesús E. Marco De Lucas, Giovanni Aloisio
	Speaker: Sandro Fiore, Euro-Mediterranean Center on Climate Change Foundation
11:40 - 12:00	"Sorting Big Data on Heterogeneous Near-Data Processing Systems"
	Erik Vermij, Leandro Fiorin, Christoph Hagleitner, Koen Bertels
	Speaker: Erik Vermij, IBM Research
12:00 - 12:20	"Finding the Critical Sampling of Big Datasets"
	José Silva, Bernardete Ribeiro, Andrew Sung
	Speaker: José Silva, Department of Informatics Engineering, University of Coimbra
12:20 - 12:40	"An Empirical Comparison of Stream Clustering Algorithms"
	Matthias Carnein, Dennis Assenmacher, Heike Trautmann
	Speaker: Matthias Carnein, University of Münster
12:40 - 13:00	"Addressing Hadoop's Small File Problem with an Appendable Archive File Format"
	Thomas Renner, Johannes Müller, Lauritz Thamsen, Odej Kao
	Speaker: Thomas Renner, Technische Universität Berli

Monday May 15 14:00 – 17:30 room: Aula Magna Storica (1st floor)

Malicious Software and Hardware in Internet of Things

Aim and Scope

Cyber-physical and smart embedded systems, already highly networked, will be even more connected in the near future to form the Internet of Things, handling large amount of private and safety critical data. The pervasive diffusion of these devices will create several threats to privacy and could open new possibilities for attackers, since the security of even large portions of the Internet of Things could be harmed by compromising a reduced number of components. The possibility of securely updating devices should be guaranteed and it should be possible to verify and assert the root of trust of components. With respect to this context we expect contributions in different areas of security in Internet of Things.

Topics of interest

- Malicious firmware design and detection
- Malware in Internet of Things applications
- Hardware root of trust
- Privacy issues of smart-home systems and complex systems
- Hardware Trojans and their effects on systems
- Hardware authentication and IP protection
- Secure communication and key-management
- Implementation attacks and countermeasures
- Emerging threats and attack vectors in the Internet of Things
- Supply chain security

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- Falk Schellenberg,
  Ruhr-Universität Bochum, Germany
- Philippe Camacho,
  Dreamlab, Chile
- Fernando Krell,
  Dreamlab, Chile

Programme

14:00-14:30 Private inter-network routing for Wireless Sensor Networks and the Internet of Things

Paolo Palmieri, Luca Calderoni and Dario Maio

14:30-15:00 A Combined Strategy for Countering Power and Fault Attacks with Information Theoretic Guarantees

Sikhar Patranabis, Debapriya Basu Roy and Debdeep Mukhopadhyay

15:00-15:30 Design of S-boxes Defined with Cellular Automata Rules

Stjepan Picek, Luca Mariot, Bohan Yang, Domagoj Jakobovic and Nele Mentens

15:30-16:00 DPA on hardware implementations of Ascon and Keccak

16:00-16:30 Coffee Break

16:30-17:30 Do we need a holistic approach for the design of secure IoT systems?

Moderator: Nele Mentens

Panelists: Mauro Conti, Giorgio Di Natale, Annelie Heuser, Thomas Pöppelmann

Tuesday May 16 11:00 – 12:40 _____room: Aula Magna Storica (1st floor)

LP-EMS Workshop
Workshop on design of Low Power EMbedded Systems

Aim and scope

Modern cyber-physical and highly networked systems impose to designers challenging and conflicting requirements. Implementing real-time high-performance systems and minimizing, contemporarily, their power consumption is not straightforward. Emergent and unpredictable behaviours require these systems to adapt at runtime to mutable conditions. Therefore, advanced modelling strategies as well as efficient design automation techniques should be capable of optimizing complex parallel applications over heterogeneous multi- and many-cores platforms. Complexity on algorithmic side and heterogeneity on hardware side are colliding system constraints, which can be tackled by adopting hw/sw co-design solutions and flexible design frameworks.

With respect to this context, contributions are expected in different fields of digital signal processing such as: telecommunication, multimedia, medical imaging, computing graphics, biomedical applications and many others!

Topics of interest

- Design of self-energy aware systems;
- Design space exploration techniques, with special emphasis on power/energy estimations and power minimization methodologies;
- Parallel/high throughput processing techniques for low-power digital signal/image processing;
- Algorithm-level optimization, low-complexity algorithm for low-power digital signal/image processing;
- MPEG Green Metadata;
- Approximate computing, low power arithmetic
- Dynamic voltage and frequency scaling, HW and SW dynamic power management.

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- Francesco Conti,
  ETH Zurich and University of Bologna
- Paolo Meloni,
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- Daniel Menard,
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  KIT – Karlsruhe Institute of Technology (DE)
- Leonel Sousa,
  IST – Instituto Superior Técnico, University of Lisbon (PT)

Programme

11:00 – 11:20 Keynote : low-power IoT platforms optimized for edge computing

Eric Flamand, Greenwaves Technologies, France

11:20 – 11:40 Improving Error Resilience Analysis Methodology of Iterative Workloads for Approximate Computing

G.A. Gillani and A.B.J. Kokkeler, University of Twente, Netherlands

11:40 – 12:00 Instruction level energy model for the Adapteva Epiphany multi-core processor,

Gabriel Ortiz, Lars Svensson, Erik Alveflo and Per Larsson-Edefors,
University of Technology, Sweden

12:00 – 12h20 On Learning the Energy Model of an MPSoC for Convex Optimization

Erwan Nogues, Daniel Menard, Maxime Pelcat, Alexandre Mercat
UEB/INSA Rennes/IETR, France

12:20 – 12:40 DCT Learning-Based Hardware Design for Neural Signal Acquisition Systems

Cosimo Aprile, Johannes Wüthrich, Luca Baldassarre, Yusuf Leblebici, Volkan Cevher
EPFL, Switzerland

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Social Programme

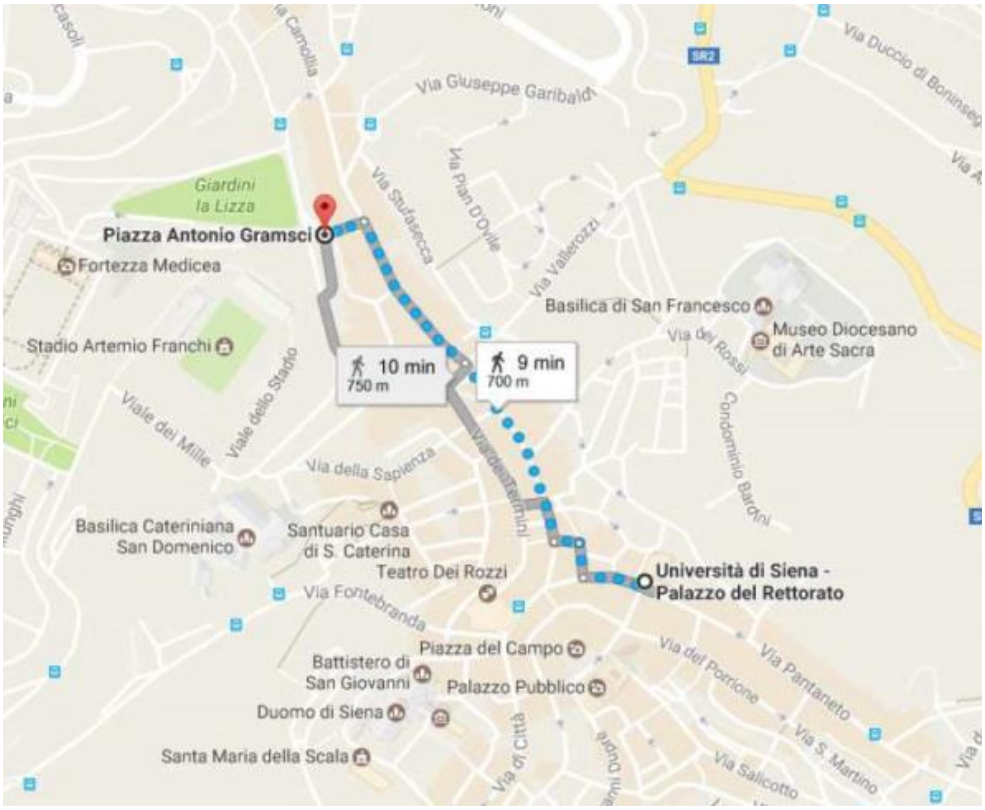
Monday May 15

17:30-19:00 **Welcome Cocktail & Poster Session**
Courtyard of the Palazzo del Rettorato of the University of Siena
Banchi di Sotto 55

Tuesday May 16

17:30 Bus departure from Piazza Gramsci
(please take note that the ticket for the dinner is required before the departure of the bus)

Guided tour and Conference Banquet
"CANTINA ANTINORI NEL CHIANTI CLASSICO"
Loc. Bargino, San Casciano Val di Pesa



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Useful Information

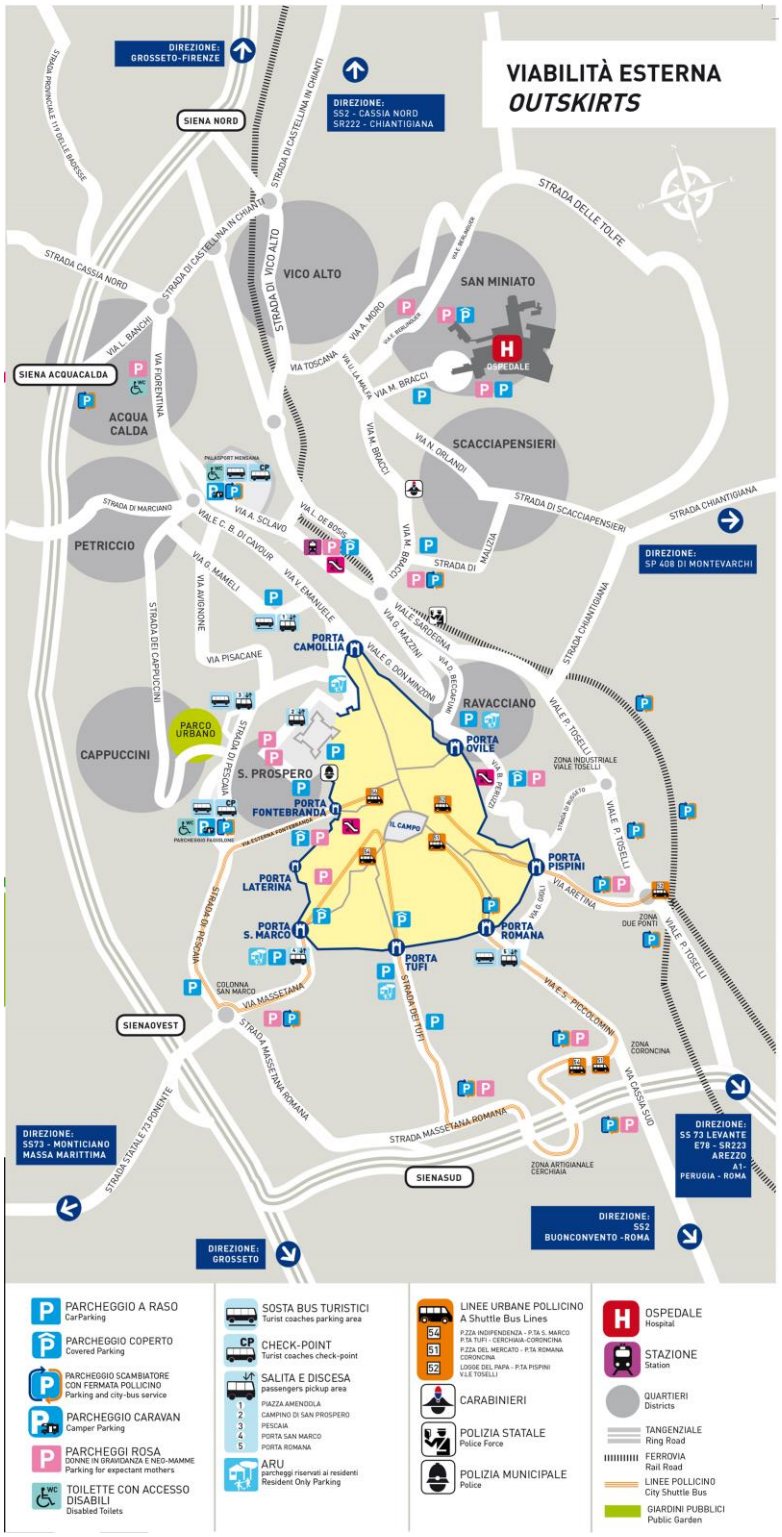
CENTRO STORICO	City center
CINTA MURARIA	City Wall
GIARDINI PUBBLICI	Public Garden
AREA PERIFERIA	City Outskirt
FERROVIA	Rail Road

- STAZIONE BUS DI LINEA — Bus Station
- RISALITA MECCANICA — Escalator
- STAZIONE — Station
- TAXI
- PRANZO AL SACCO (TARTARUGONE) — Pic-nic area
- BAGNI PUBBLICI — Toilets
- FONTI — Fountains
- INFORMAZIONI — Information
- OSPEDALE — Hospital
- POLIZIA STATALE — Police Force
- POLIZIA MUNICIPALE — Police
- CARABINIERI
- CHIESA — Church
- SINAGOGA — Sinagogue
- PARCHEGGI ROSA — DONNE IN GRAVIDANZA E NEO-MAMME — Parking for expectant mothers
- PARCHEGGIO A RASO — Parking
- PARCHEGGIO COPERTO — Covered Parking
- ARU — PARCHEGGI RISERVATI AI RESIDENTI — Resident only Parking

LUOGHI D'INTERESSE
Place of Interest

1. CHIESA DI SAN PIETRO ALLA MAGIONE
2. FONTI DI PESCAIA MUSEO DELL'ACQUA
3. PIAZZA SALIMBENI
4. FORTEZZA MEDICEA ENOTECA ITALIANA FONDAZIONE SIENA JAZZ
5. BASILICA DI SAN FRANCESCO
6. CHIESA DI SANTA MARIA IN PROVENZANO
7. BASILICA DI SAN DOMENICO
8. SANTUARIO-CASA DI SANTA CATERINA
9. LOGGIA DELLA MERCANZIA
10. PIAZZA DEL CAMPO MUSEO CIVICO TEATRO COMUNALE DEI RINNOVATI
11. SINAGOGA
12. PALAZZO PICCOLOMINI ARCHIVIO DI STATO
13. LOGGE DEL PAPA CHIESA DI SAN MARTINO
14. BASILICA DI SANTA MARIA DEI SERVI
15. PALAZZO CHIGI SARACINI ACCADEMIA MUSICALE CHIGIANA
16. PIAZZA DUOMO CATTEDRALE DI SANTA MARIA ASSUNTA MUSEO DELL'OPERA DELLA METROPOLITANA COMPLESSO MUSEALE SANTA MARIA DELLA SCALA
17. PINACOTECA NAZIONALE
18. ACCADEMIA DEI FISIOCRITICI
19. ORTO BOTANICO

COMUNE DI SIENA



EMERGENZA MEDICA
Emergency Medical Care
✆ 118

CARABINIERI ✆ 112

POLIZIA DI STATO
Police Force ✆ 113

POLIZIA MUNICIPALE
Police ✆ 0577 292550

VIGILI DEL FUOCO
Fire Department ✆ 115

QUESTURA/PREFETTURA
Central Police Station-
Prefecture ✆ 0577 201111

TAXI ✆ 0577 49222

SIENA PARCHEGGI
Siena Parcheggi Management
Parking ✆ 0577 228711

UNIVERSITÀ DEGLI STUDI DI SIENA (Rettorato)
University ✆ 0577 232111

MUSEI COMUNALI
Museum
TORRE DEL MANGIA
MUSEO CIVICO
SANTA MARIA DELLA SCALA
✆ 0577 292615-614
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